UNDERSTANDING & APPLYING THE ANALOG SWITCH

INTRODUCTION

Historically the analog switch has been thought of as a solid state relay, and many of its common applications are areas where the relay dominated the scene a few years ago. Routing signals in telephone exchanges is the most obvious example. More recently, however, as creative designers are becoming aware of the unique properties of the analog switch, a new generation of applications is emerging which were simply not possible using relays. The ability to change the gain of an amplifier, or the time constant of an integrator, in less than a microsecond has far-reaching implications in real-time analog signal processing.

The purpose of this note is twofold. Firstly, to act as an introduction to analog switches to those who have hitherto only used relays. Secondly, to compare and contrast the features of the different switch families and to illustrate their use with practical applications.

RELAYS AND THE ANALOG SWITCH

Since the class of relay closest to the analog switch in terms of cost and packaging is the reed relay, the comparison which follows is confined to this type of device. Reed relays have three advantages; they are easy to apply (current through a coil opens or closes isolated contacts), they will handle signals of the order of hundreds of volts, and their ON-resistance is low. So what does the solid-state analog switch have to offer? It outperforms the mechanical relay in almost every other specification. It is much faster, does not suffer from contact bounce problems, is more rugged since there are no moving parts, has several times the number of switches per package, and is easier to drive since the switch can interface directly with TTL without requiring back-EMF diode protection, etc. The salient features of the two switch types are given in Table 1.

Analog switches can be thought of in terms of form A, B, and C relays; it is only necessary to add some external connections as shown in Table 2. The table shows devices from the IH5040 series, with the switch states for a logic "1" input. In the normal state (logic "0" input) the contact closures drawn as closed would be open and vice versa.

TABLE 1

PARAMETER \ FAMILY	TYPICAL REED RELAY	HYBRID FET & BIPOLAR SWITCH (IH5001)	C-MOS SWITCH (IH5040)	VIRTUAL GROUND SWITCH (IH5009)	POSITIVE SIGNAL SWITCH (IH5025)
SIGNAL HANDLING (V_S = ±15V WHERE APPLICABLE)	±300V	±8V	±14V	±15V (NOTE 1)	0V TO +10V (NOTE 2)
ON RESISTANCE	0.1Ω	30Ω	75Ω	100Ω	100Ω
SPEED (t_{on}/t_{off})	1000/500μs	0.5/1.0μs	1.0/0.5μs	0.5/0.5μs	0.2/0.2μs
LOGIC COMPATIBILITY	NO	YES	YES	YES	YES
STEADY STATE QUIESCENT CURRENT (WHEN ON)	10mA @ 15V	3.5mA	0.1mA	NONE	NONE
COST PER CHANNEL @ 1000 PCS	$3.00	$4.00	$2.50	< $1.00	< $1.00

NOTE 1: When used as recommended at the virtual ground point of an operational amplifier.
NOTE 2: A method of switching +20V signals is explained in the data sheet.

THE AVAILABLE SWITCH TYPES

There are basically four different switch types on the market at the present time. They may be summarized as follows:

a. Combination FET (MOS or Junction) and bipolar hybrid designs.
b. Monolithic C-MOS Designs.
c. Simple low-cost J-FET "virtual ground" designs.
d. Simple low-cost "positive signal" designs.

a. Combination FET and Bipolar Hybrid Designs

These may be described as first generation single package analog switches. In many respects they are equivalent to the μA709 in the op-amp world; both deserve credit for pioneering the concept of a complete building block in a single package, and yet both have been outdated by advancing technologies and design concepts.

This family is of hybrid construction and consists of a Bipolar, monolithic driver chip and MOSFETs or junction

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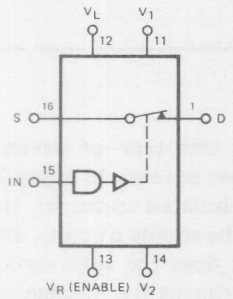
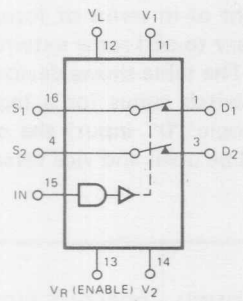
TABLE 2: RELAY EQUIVALENT CONTACT FORMS

NOTE 1: Switch states are for logic "1" input
NOTE 2: Pin Connections are for DIP package

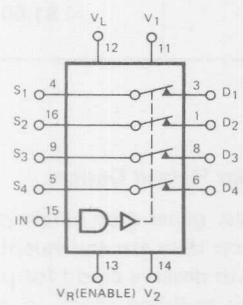
FORM A



SPST
IH5040 (R_{DS} (ON) <75Ω)

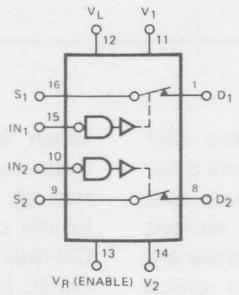


DPST
IH5044 (R_{DS} (ON) <75Ω)

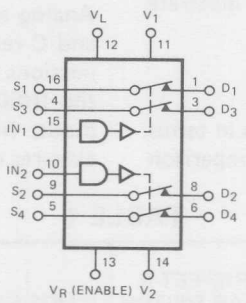


4PST
IH5047 (R_{DS} (ON) <75Ω)

DUAL A

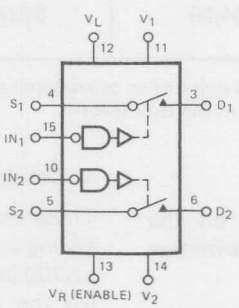


DUAL SPST
IH5041 (R_{DS} (ON) <75Ω)



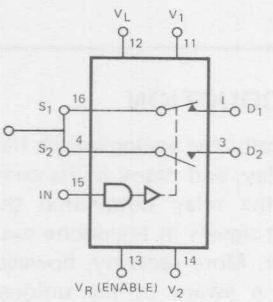
DUAL DPST
IH5049 (R_{DS} (ON) <30Ω)
IH5045 (R_{DS} (ON) <75Ω)

DUAL B

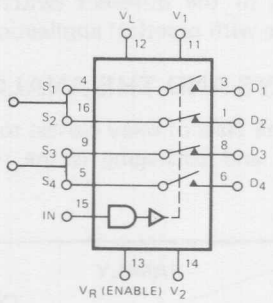


DUAL SPST
IH5048 (R_{DS} (ON) <30Ω)

FORM C

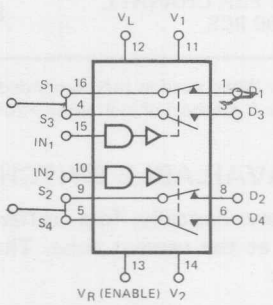


SPDT
IH5050 (R_{DS}(ON) < 30Ω)
IH5042 (R_{DS}(ON) < 75Ω)



DPDT
IH5046 (R_{DS} (ON) <75Ω)

DUAL C



DUAL SPDT
IH5051 (R_{DS} (ON) <30Ω)
IH5043 (R_{DS} (ON) <75Ω)

FETs as output devices. The driver stage is required to translate the TTL voltage levels to those suitable to drive the output stage; this is typically a 3V to +15V or a 0.8V to –15V translation.

The DG111 through DG125 grouping has a bipolar driver and a P-MOS monolithic output stage, with up to six (6) independent MOSFETs on each chip (Fig. 1). These are enhancement mode MOSFETs and are turned off with no power applied. The range of switching is ±10V with +20V and –10V power supplies. Typical $R_{DS(on)}$ is 70Ω for +10V signals, 150Ω for low level signals and about 300Ω for –10V signals. Notice the switch does not show a constant impedance as signal level is varied. To minimize this modulation effect by the signal, these parts should work into relatively high load resistances (i.e., $R_L \geq 10K\Omega$).

The DG126 through DG164 family, and also the IH5001 through IH5007, again have a bipolar driver chip for voltage translation, but discrete J-FET chips are used as output stages here (Fig. 2). Typical $R_{DS(on)}$'s are in the 5Ω to 50Ω range (depending on Part #), and all are characterized by a constant switch resistance. Typical analog switching levels are ±8V with ±15V supplies.

For both of the above families, the following are common characteristics:

1. Construction is hybrid.
2. Switching speeds are typically 0.3 μS and 1.0 μS (t_{on} and t_{off})
3. Leakages are in 1 nA range.
4. Charge injections are very similar.
5. Circuit power dissipation is very similar.

The new monolithic C-MOS analog switches discussed in the next section will outperform these earlier hybrids in almost every parameter, will ultimately be much less costly to manufacture, and will undoubtably become the 741's and 101A's of the analog switch world.

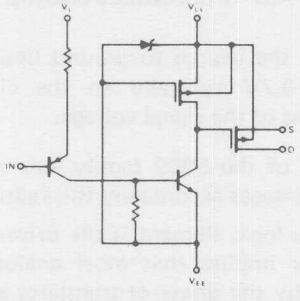


FIGURE 1. DG118 (ONE CHANNEL)

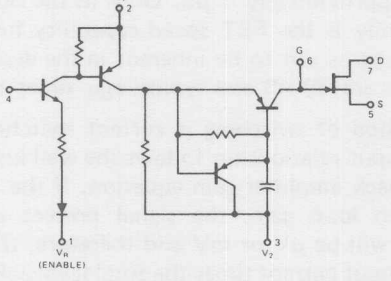


FIGURE 2. IH5001

b. Monolithic C-MOS Designs

For all new designs, the C-MOS switches should be considered along with the more specialized types described in c. and d. It will be shown later that the C-MOS switch is extremely versatile; in fact, the only reason *not* to use it is in those instances where the much simpler (and less costly) specialized circuits can perform the task.

These switches are of monolithic construction and include part #'s IH5040 through IH5052. Each part is a complete driver and output stage combination and the family has the following salient features:

1. TTL compatible.
2. Switches up to ±14V with ±15V supplies.
3. Has overvoltage protection to ±25V signal inputs.
4. Draws <100 μA (1 μA typ.) from ±15V supplies.
5. Break-before-make switching with typical $t_{on} \approx 500$ nS and typical $t_{off} \approx 250$ nS.
6. $R_{DS(on)} < 75\Omega$.
7. Improved reliability due to lower power consumption and monolithic construction.

The use of C-MOS processing allows the fabrication of a family of switches with superior parameters compared with the older hybrid techniques. For example, the C-MOS parts can switch within 1V of power supplies (±14V with ±15V supplies) while parts in group a) switch ±8V with ±15V or ±10V with +20V and –10V typically. Also, the C-MOS quiescent current is typically microamperes instead of milliamperes; thus it is ideal for portable equipment. C-MOS is compatible with any logic, while the hybrid families are strictly designed for TTL (+5V logic).

The C-MOS switches are offered in a variety of switch configurations, i.e., SPST, DUAL SPST, DPST, DUAL DPST, DPDT, 4PST, etc. Each different part is merely a metal mask option of the basic C-MOS device. A typical schematic is shown in Fig. 3.

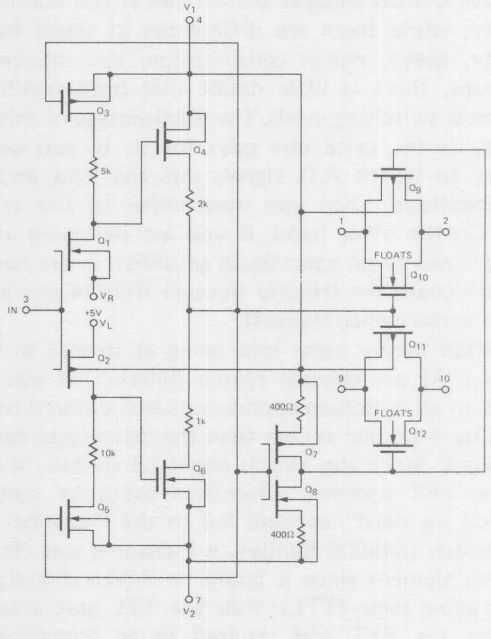
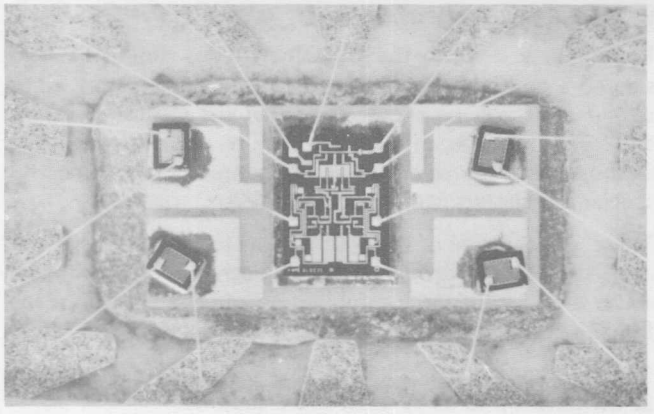
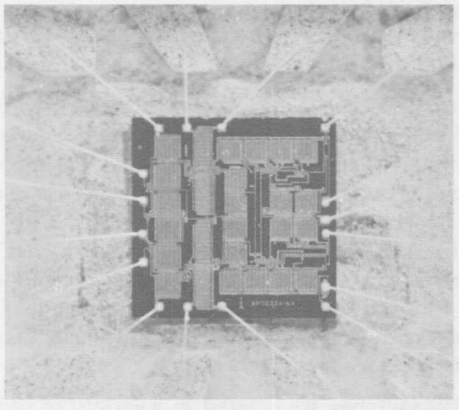


FIGURE 3. IH5042 SCHEMATIC



A. HYBRID ANALOG GATE USING MONOLITHIC BIPOLAR DRIVERS AND FET SWITCHES.



B. MONOLITHIC C-MOS ANALOG GATE.

c. Virtual Ground Switch Family

The *Combination FET and Bipolar Hybrid Designs and Monolithic C-MOS Designs* are families which feature great versatility; while there are differences in signal handling capability, speed, power consumption, etc., between the two groups, there is little doubt that both families will handle most switching needs. The disadvantage of this added versatility is the price one pays for it. If you need the flexibility to switch A.C. signals into any load, and up to ±10V amplitude, then you need either of the a) or b) groups. On the other hand, if you are switching into the inverting input of an operational amplifier, or are switching low level signals, the IH5009 through IH5024 provides the best cost performance tradeoff.

The IH5009 family came into being at Intersil to fill the need for a $1 per channel switch function. It was found that 40% of all switching applications encountered could be satisfied by a simpler switch than the driver/gate combination designs. Since the switch could be simpler, the costs were less and customer objectives could be met. This "designing for need" concept led to the P-channel J-FET analog switch (IH5009 family). A P-channel was chosen as the gating element since it could be driven directly from positive going logic (TTL); thus the TTL gate acted as a driver for the FET and resulted in an immediate cost saving to end users, since previous designs had required a separate driver.

The phrase low level switching is a misnomer as applied to the IH5009 family of "virtual ground switches" (the negative feedback point of an op amp is a virtual ground). In reality, the switch could handle ±100V if one could find an op amp capable of ±100V output swings, since the signal appearing at the virtual ground is attenuated by the open loop gain. When the switch is off, it is the diodes that limit the swings, at the J-FET, to levels compatible with the logic.

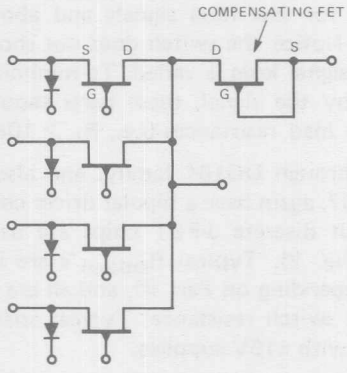


FIGURE 4. IH5009 SCHEMATIC

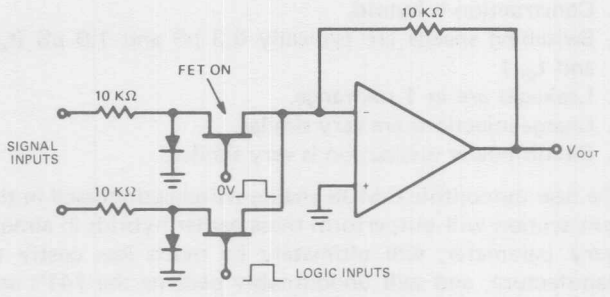


FIGURE 5. SWITCHING AT VIRTUAL GROUND OF AN OP-AMP (2 CHANNELS SHOWN)

The diodes from the source to ground limit the swing at the J-FET to +0.7V typically so the circuit operates correctly regardless of the signal voltage.

While the intent of the 5009 family was to reduce cost, some unique advantages accompany this reduction:

1. Since the TTL logic element is the driver, the switch is very fast; this implies that most analog switches are speed limited by the driver or translator and this is true. If the driver takes 1 μS to switch from +15V to –15V then t_{off} time of driver-gate combination (N-channel) will be approximately 1 μS. Only in the 5009 and the 5025 family is the FET speed capability fully utilized; this then turns out to be inherent in the design. Typical t_{on} times are 50 nS and typical t_{off} times are 150 nS.
2. The method of switching is current switching and the output/input relationship follows the well known inverting feedback amplifier gain equation. If the op amp has high open loop gain, the signal present at summing junction will be μV or mV and therefore, the output is just the input current times the total feedback resistance. Thus, for 0.1% or 0.01% switching accuracy, a feedback J-FET is used in series with the feedback resistor (R_f);

this feedback FET compensates for the error due to I_{in} x R_{DS} loss at the input (R_{DS} = "on" resistance of P-JFET). In the 5009 family, a "compensating FET" is included in the package specifically for this purpose (Fig. 6). The two FETs track so the gain tracks through temperature and system accuracy can be maintained.

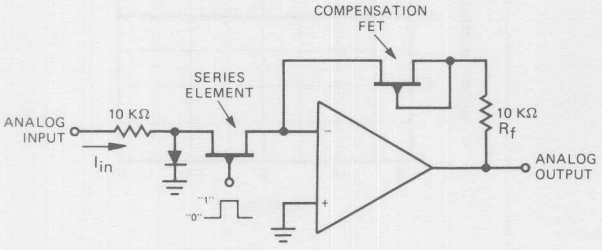


FIGURE 6. USE OF "COMPENSATING FET" TO REDUCE $R_{DS(ON)}$ ERROR

The 5009 series is broken up into two different groups. All the odd-numbered parts (5009, 5011, etc.) are designed to be used with TTL open collector logic (+15V power supply) while the even-numbered ones are designed to be used with +5V TTL logic. For odd-numbered parts, the J-FETs have a pinch-off voltage of 4V to 10V and a maximum $R_{DS(on)}$ of 100Ω (65Ω typical) and the even numbers have a pinch-off range of 2V to 3.9V and a maximum $R_{DS(on)}$ of 150Ω (90Ω typical).

For both even and odd numbers, the match between any two channels is better than 50Ω and versions at 25Ω, 10Ω, 5Ω are available at increased cost over the basic 50Ω match. Additional information on the 5009 series is given in Intersil Application Note A004 "The IH5009 Series of Low Cost Analog Switches."

d. Positive Signal Switch Family

Just as the 5009 series fits a particular need for virtual ground switching applications, the IH5025 through IH5038 fits into a certain niche when only positive signals are switched. The 5025 series has been designed to switch any signal from 0V to +10V using TTL open collector logic (+15V power supply). Signals up to +25V can be switched

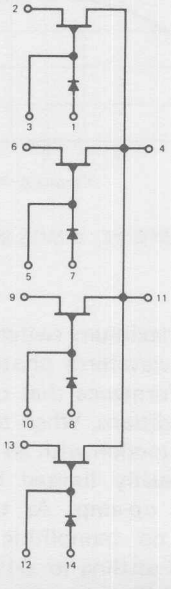


FIGURE 7. IH5025 SCHEMATIC

by using a +30V supply at open collector terminal point. There is no restriction on the load, as in the 5009 family, and load resistances from 50Ω to infinity are easily handled. A typical switching circuit is shown in Fig. 8 below:

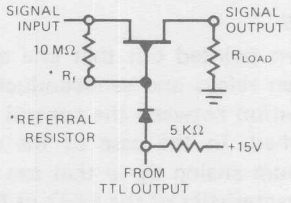


FIGURE 8. TYPICAL SWITCHING CIRCUIT (ONE CHANNEL)

Notice that no op amp is required to be part of the switching circuit, as is the case in the 5009 family. The disadvantage of this series is that negative signals cannot be switched unless external parts are added as in Fig. 9.

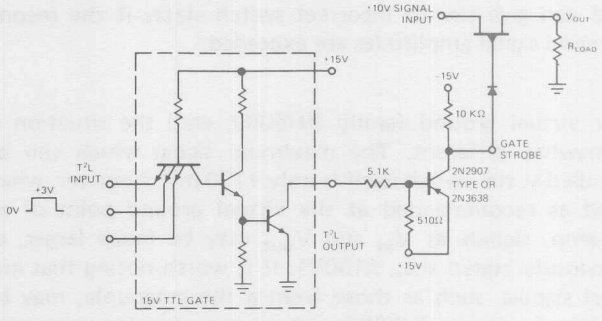


FIGURE 9. SWITCHING BIPOLAR SIGNALS USING THE IH5025

Thus, by adding a PNP (2N3638 or 2N2907, etc.) and two resistors, the 5025 family becomes just as versatile as any other analog switch. Of course, open collector logic must still be used. When switching only positive signals, so that the circuit is driven directly from logic, speed is very fast; in fact, $t_{(on)} \approx 50$ nS and $t_{(off)} \approx 200$ nS up to R_L = 1K loads ($C_L \leqq 10$ pF). When driving through PNP stage shown, speed is considerably reduced (to 300 nS, 1 μS for $t_{(on)}$, $t_{(off)}$ respectively).

The 5025 family is broken up into 2 distinct groups, all of which have a pinch-off range of 2V to 3.9V. The odd-numbered parts have a maximum $R_{DS(on)}$ of 100Ω and the even numbers have a maximum of 150Ω; the difference between the two groups is that a larger geometry FET is used for odd-numbered parts. This larger geometry, while producing a lower on resistance, also inherently has about twice the charge injection when compared with the even-numbered parts. This is specified at 20 mV maximum into 10,000 pF for all parts. Typical charge injections are 7 mV for even-numbered parts and 14 mV for odd-numbered parts.

As with the 5009 family, the 5025 series has a channel to channel $R_{DS(on)}$ match of 50Ω or less, with typicals running in the 25Ω area.

While the 5025 family has been targeted for use with TTL open collector logic, it can be used with 5V logic under the restraint that a maximum of 1V signal is switched. While this is rather restrictive, there are a few applications where this 1V maximum would be no problem; i.e., when switching transducer signals directly.

COMPARING THE PARAMETERS

Table 1 compares the key features of different switch types. A more detailed description of specific parameters follows:

A. Signal Handling

It has already been pointed out that one of the primary differences between relays and semiconductor switches is the degree of isolation between the control signal and the signal being switched. In the case of the semiconductor switch, the maximum analog signal that can be handled is related to the characteristics of the FETs or MOSFETs, and the supply voltages. When the switch itself is an N channel J-FET, which in the absence of any gate bias is in the ON state, the device is held off by driving the gate towards the negative supply. Clearly, if the potential on the drain or source comes within V_p (the pinch-off voltage) of the gate, the device will turn on. With MOSFETs an analogous situation exists: The analog signal modulates the gate bias and can give rise to incorrect switch states if the recommended signal amplitudes are exceeded.

For virtual ground family (IH5009, etc.) the situation is somewhat different. The maximum signal which can be handled at the switch itself is only +700 mV; however, when used as recommended at the virtual ground point of an op-amp, signals at V_{in} and V_{out} may be much larger, as previously stated (i.e., ±100V). It is worth noting that low level signals, such as those from a thermocouple, may be switched using an IH5009 without the need for an op-amp provided the amplitudes are less than 700 mV.

B. ON Resistance

The ON-resistance of a good reed relay is substantially less than that of a typical analog switch. However, the widespread use of high input-impedance op-amp buffers has tended to decrease the importance of ON-resistance as a key parameter. It is almost always possible to design the circuitry interfacing with the switch so that an ON-resistance of 30Ω to 100Ω does not contribute a substantial error. Some of these techniques are illustrated in the applications given on pages 10 through 16.

In the case of the IH5009 series, the effective ON-resistance of the switches may be further reduced by use of the "compensating FET" as described earlier.

The linearity of ON-resistance as a function of the analog signal is dependent on the switch type. For junction FET switches, which are normally on, $R_{DS(on)}$ is independent of the analog signal (Fig. 10). For P-MOS switches, a negative gate bias is required to turn the device on. The analog signal thus modulates the bias voltage, giving rise to the characteristics seen in Fig. 11. In the case of the C-MOS switch, the $R_{DS(on)}$ of the "p" and the "n" channel in parallel tend to compensate, as shown in Fig. 12.

The temperature characteristics of the different switch types are shown in Fig. 13 through 15.

r_{DS}(ON) AS A FUNCTION OF THE ANALOG SIGNAL VOLTAGE

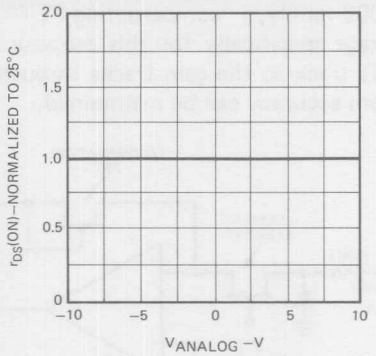


FIGURE 10. J-FET SWITCH

r_{DS}(ON) AS A FUNCTION OF THE ANALOG SIGNAL VOLTAGE

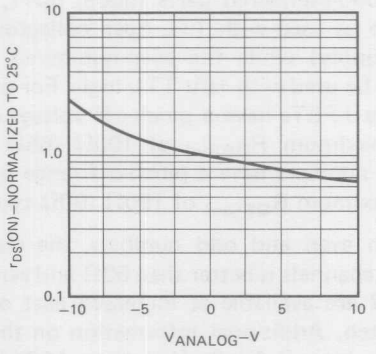


FIGURE 11. P-MOS SWITCH

r_{DS}(ON) AS A FUNCTION OF THE ANALOG SIGNAL VOLTAGE

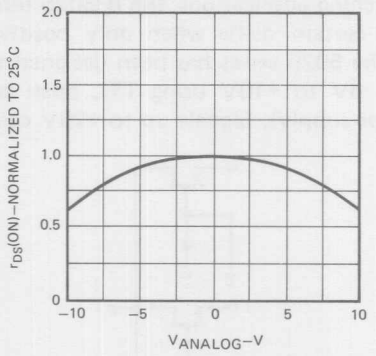


FIGURE 12. C-MOS SWITCH

C. Speed

Table 1 shows the maximum switching times for various switch families. The waveform photos which follow illustrate the typical performance that can be expected under normal operating conditions. When the 5009 and the 5025 series are used in conjunction with an op-amp, the switching characteristics are usually limited by the slew rate and settling time of the op-amp. At the present time, for example, there are no monolithic op-amps capable of swinging 10 volts and settling to .01% in less than 500 nS, even though the IH5009 is capable of such performance.

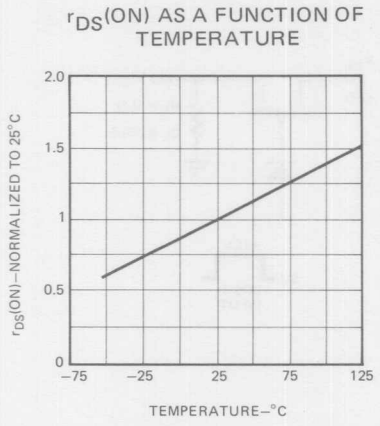


FIGURE 13. J-FET SWITCH

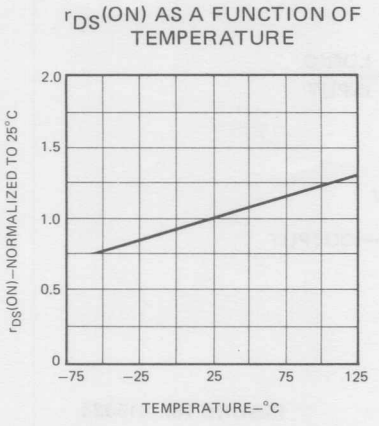


FIGURE 14. P-MOS SWITCH

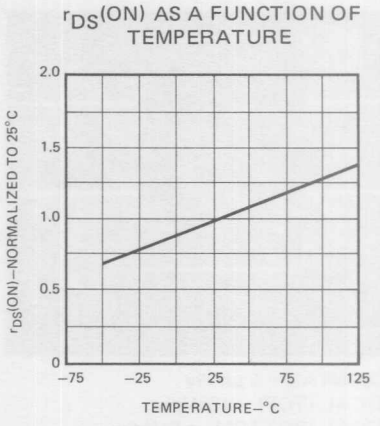
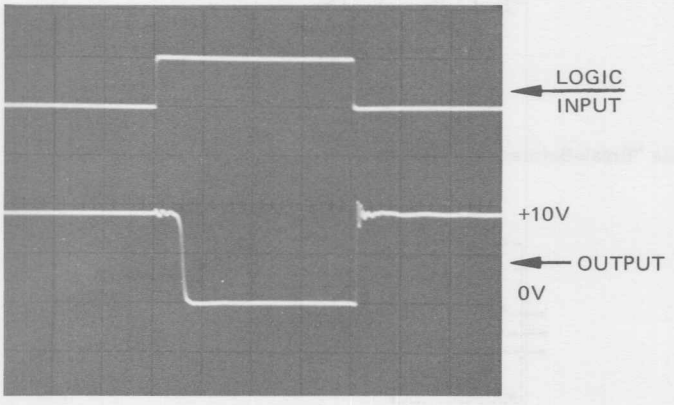


FIGURE 15. C-MOS SWITCH

TYPICAL SWITCHING WAVEFORMS



HORIZONTAL = 1 μs/div
VERTICAL = 5V/div

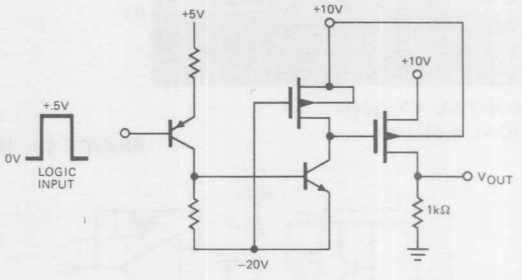
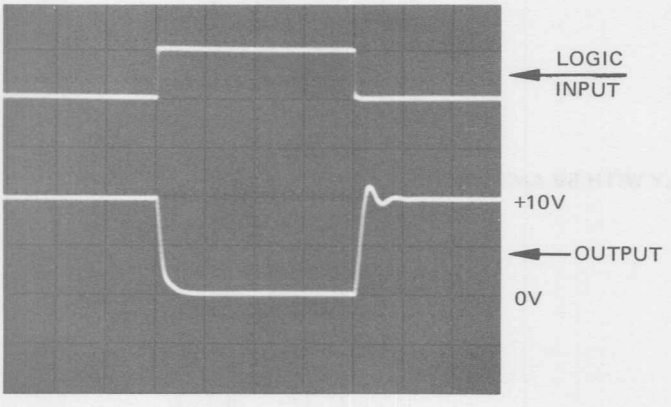


FIGURE 16. DG118 (Note "Make-Before-Break" Action)



HORIZONTAL = 1 μs/div
VERTICAL = 5V/div

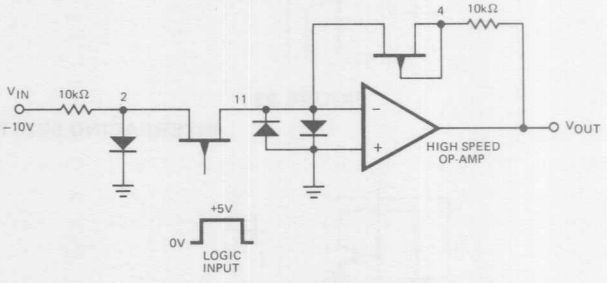
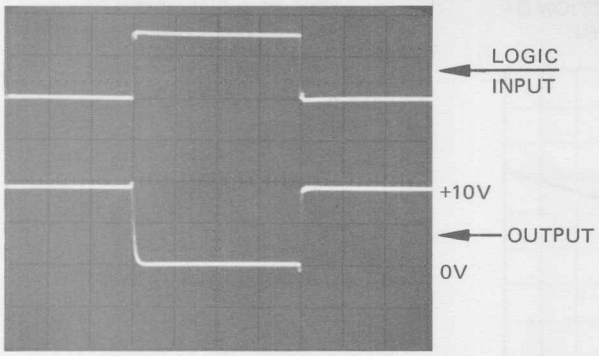
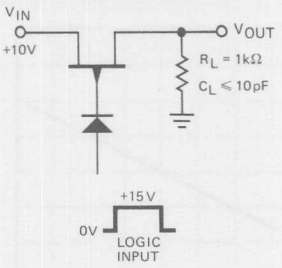


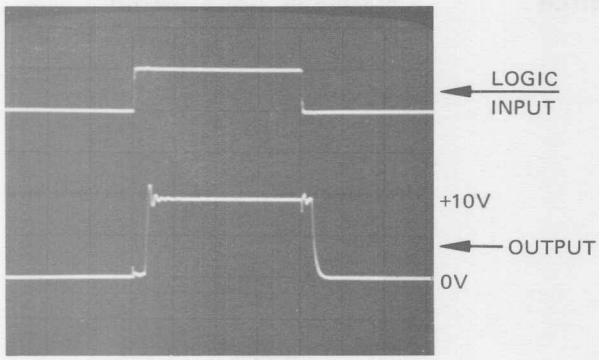
FIGURE 17. IH5010

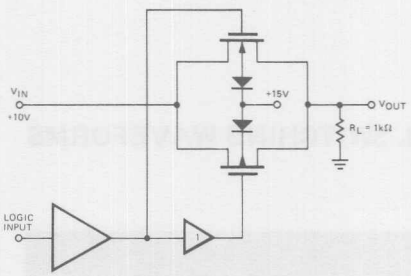




HORIZONTAL = 1 μs/div
VERTICAL (TOP) = 10V/div
VERTICAL (BOTTOM) = 5V/div

FIGURE 18. IH5025





HORIZONTAL = 1 μs/div
VERTICAL = 5V/div

FIGURE 19. IH5041 (Note "Break-Before-Make" Action)

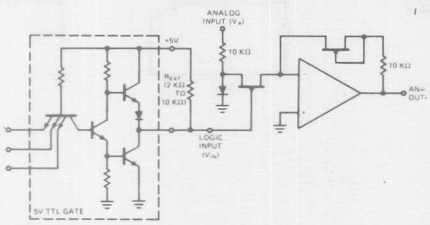


FIGURE 20.

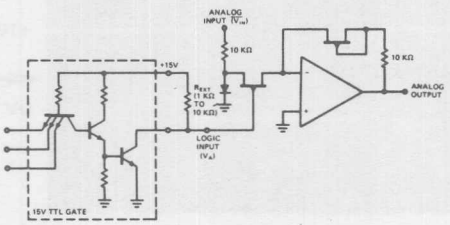


FIGURE 21.

INTERFACING 5009 FAMILY WITH 5V AND 15V TTL

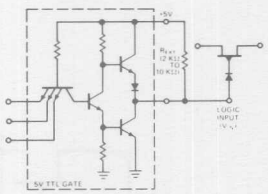


FIGURE 22

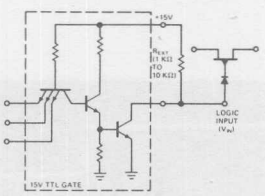


FIGURE 23

INTERFACING 5025 FAMILY WITH 5V AND 15V TTL

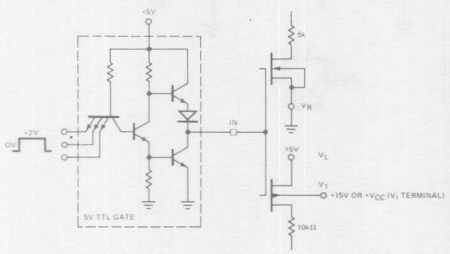


FIGURE 24

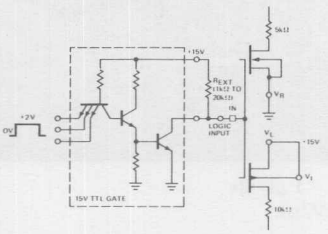


FIGURE 25

INTERFACING 5040 FAMILY WITH 5V AND 15V TTL

D. Logic Compatibility

All the popular solid state switches are compatible with TTL output swings; some require a pull-up resistor to guarantee correct operation however. Schematics showing how to interface with both standard (5V) TTL and high level open collector (15V) are given in Fig. 20 through 25.

E. Power Supplies

The IH5009 and IH5025 require no external supplies; the only power used is gate leakage current drawn from the logic. The IH5040 C-MOS circuits require ±15 volts and +5 volts, but again the only steady state power drain is a leakage current of 1 μA typical. The hybrid switches utilizing bipolar drivers require ±15 volt supplies, and typically use 2 mA in the ON condition. In the OFF state this current is much reduced and may only consist of a few microamps.

F. Charge Injection

Most analog switches exhibit some degree of charge injection, due to capacitive coupling between the FET gate and the channel. This is a difficult parameter to define in quantitative terms since it depends on the rate of change of the gate drive signal.

However, it turns out that all the analog gates under discussion in this note exhibit similar charge injection characteristics. Using the IH5025, for example, in the test circuit of Fig. 26, the waveform at the output is as shown in Fig. 27. Note that the equivalent circuit of Fig. 26 is simply a capacitance divider between the gate-channel capacitance and the load capacitance. For other operating conditions, the amplitude of the charge injection spike can be scaled proportionately. For example, doubling the size of the load capacitance will halve the spike amplitude.

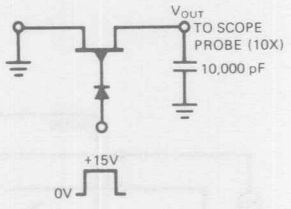
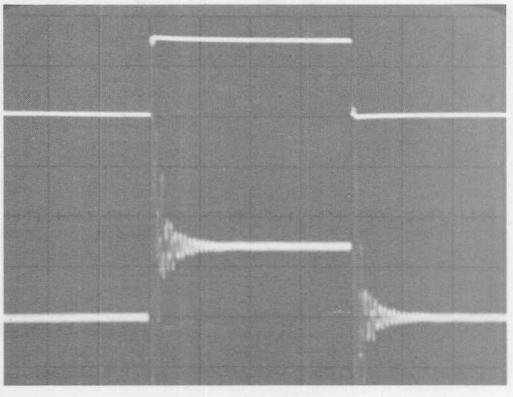


FIGURE 26. CHARGE INJECTION TEST CIRCUIT



UPPER WAVEFORM = LOGIC INPUT (10V/div)
LOWER WAVEFORM = OUTPUT (5 mV/div)
HORIZONTAL = 1.0 μs/div

FIGURE 27. IH5025 CHARGE INJECTION

SUMMARY

As a guide to users trying to decide which of Intersil's family of analog gates is most appropriate for their system needs, the following summary may help to narrow the choice:

Use	Intersil Family & Key Features
Any portable equipment	IH5040 CMOS family. Lowest power dissipation (25 μW typ.). Compatible with CMOS logic levels.
Telephone switching	IH5009 or IH5025 family. Very fast switching to allow multiplexing many signals over the same line; lowest cost part.
Computer interfacing equipment (Disc readouts. Read and write circuits from memory drums, etc.)	IH5009 or IH5025 family for low cost.
Video or radar switching	IH5025 family for fastest speed.
Military Avionics	
a. Ground support material	DG116 thru DG164 family or IH5040 family when versatility is more important than cost.
b. Airborne equipment	IH5040 family for minimum waste of power and versatility to perform many different switching functions with the same part.
Any switching done in conjunction with operational amplifiers (i.e., switched integrators, switched gain, integrating sample and hold, etc.)	IH5009 family can be switched directly from logic in virtual ground applications.
Any system requiring switch to be off when power is off	DG116 thru DG125 family or IH5050 family. MOSFET and CMOS devices require power to be turned on.

APPLICATIONS – DG120 SERIES

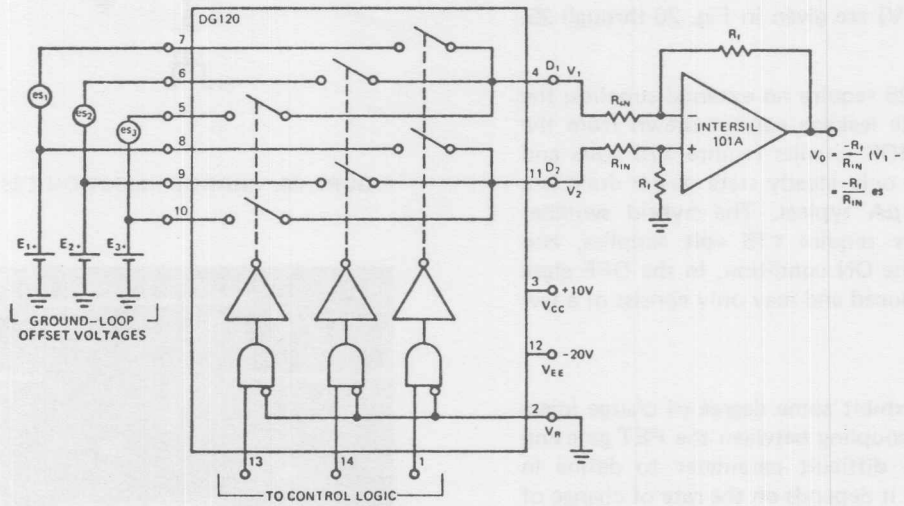


FIGURE 28. 3-CHANNEL DIFFERENTIAL MULTIPLEXER

APPLICATIONS – IH5009 SERIES

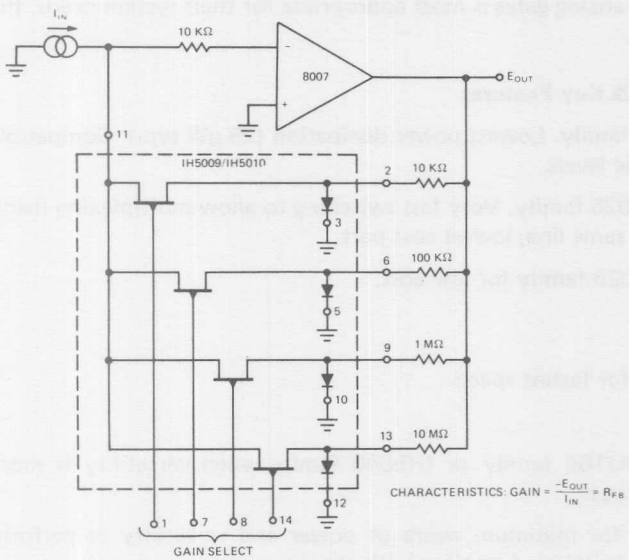


FIGURE 29. GAIN PROGRAMMABLE AMPLIFIER

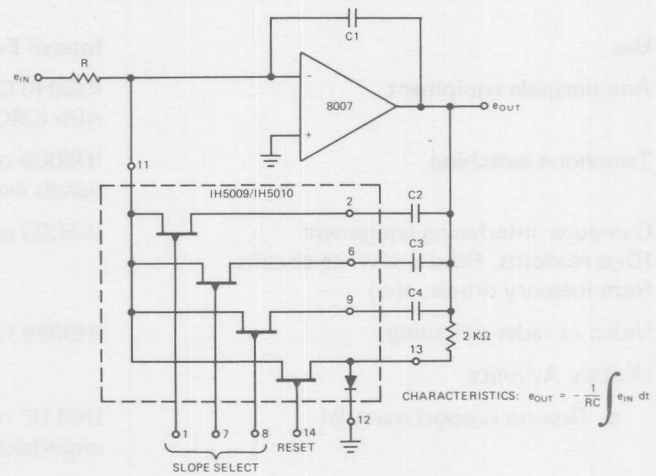


FIGURE 30. PROGRAMMABLE INTEGRATOR WITH RESET

APPLICATIONS – IH5009 SERIES (Cont.)

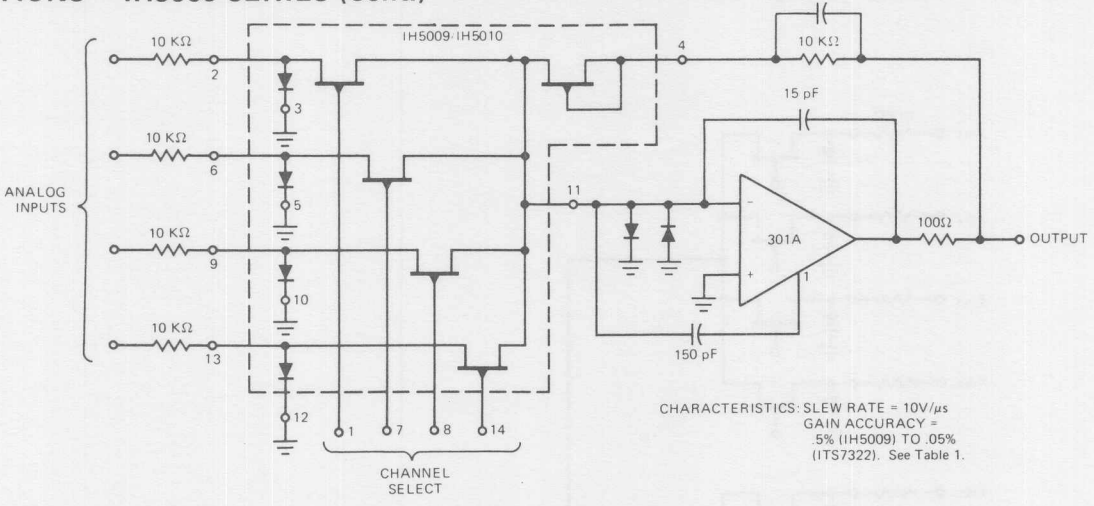


FIGURE 31. LOW COST 4 CHANNEL MULTIPLEXER

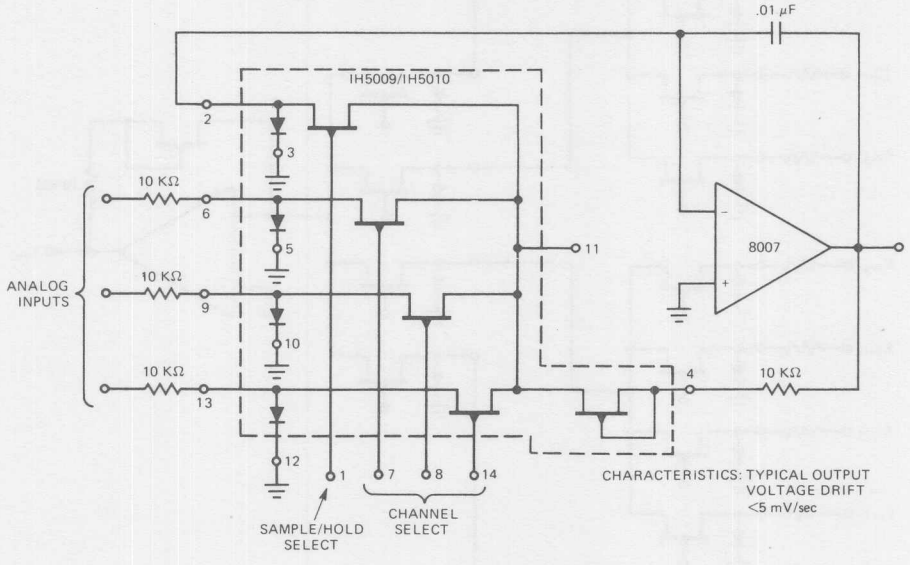


FIGURE 32. 3 CHANNEL MULTIPLEXER WITH SAMPLE & HOLD

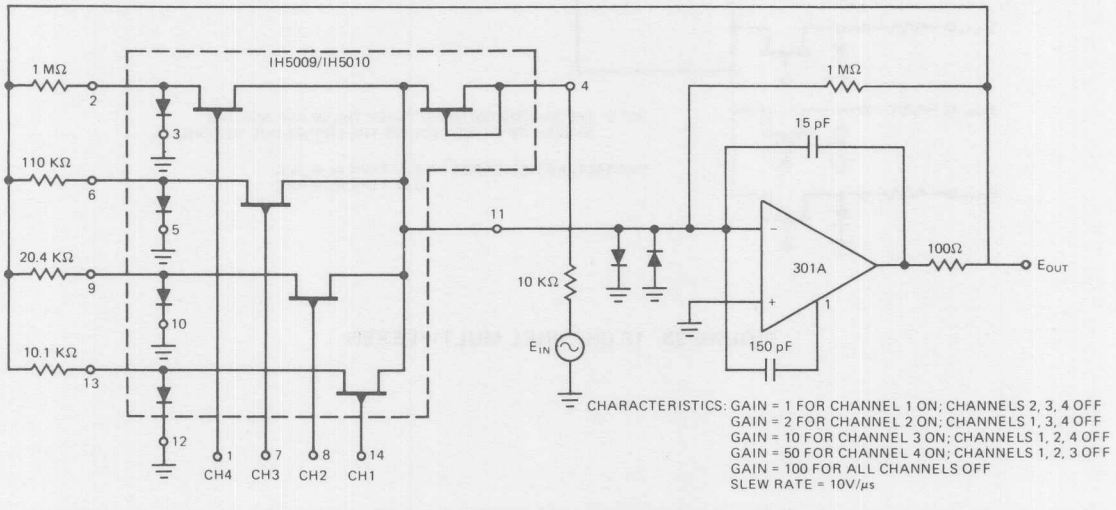


FIGURE 32. GAIN RANGING CIRCUIT

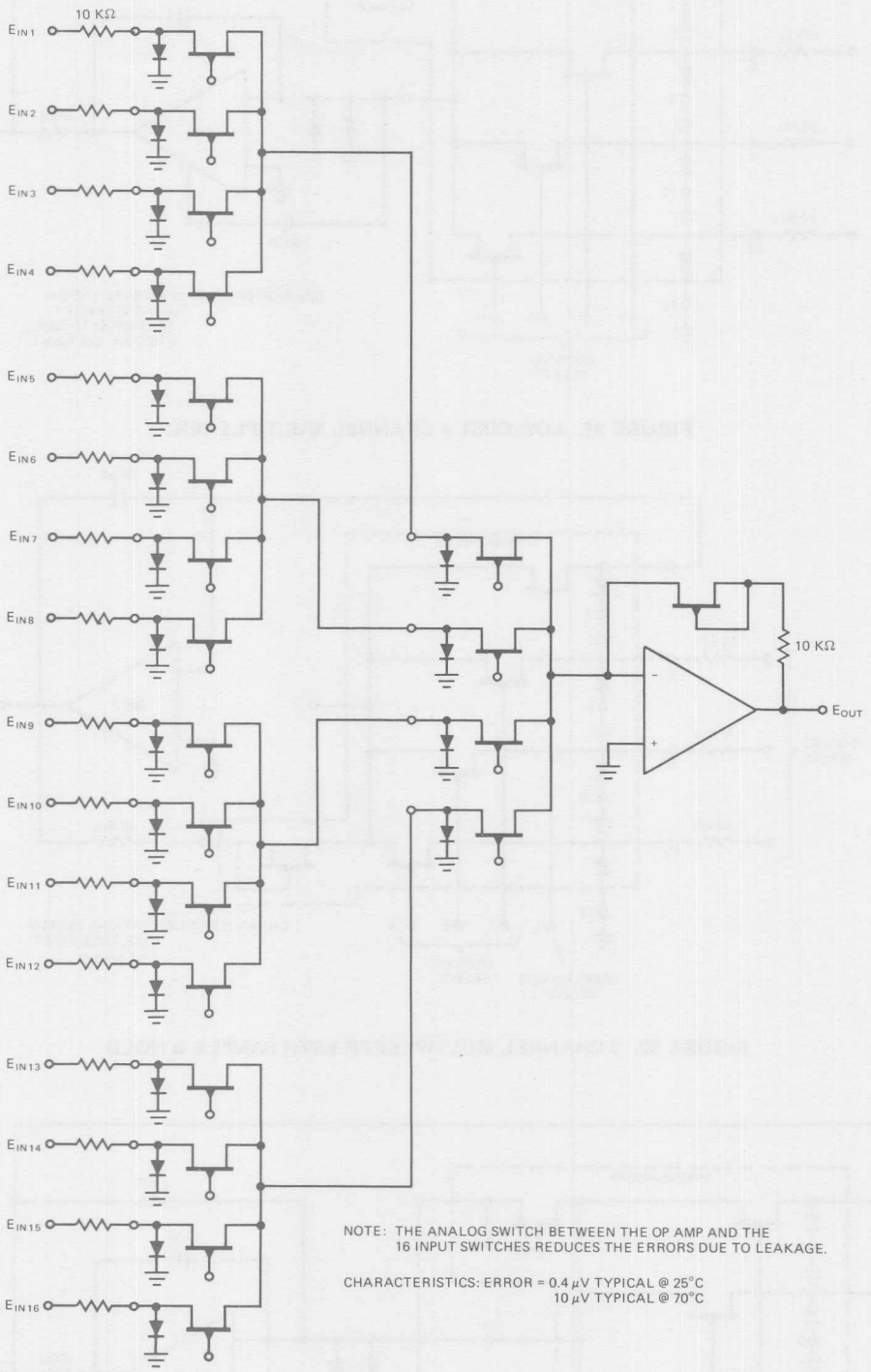


FIGURE 33. 16 CHANNEL MULTIPLEXER

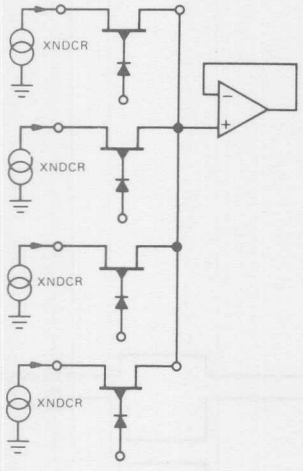


FIGURE 34. MULTIPLEXER FROM POSITIVE OUTPUT TRANSDUCERS

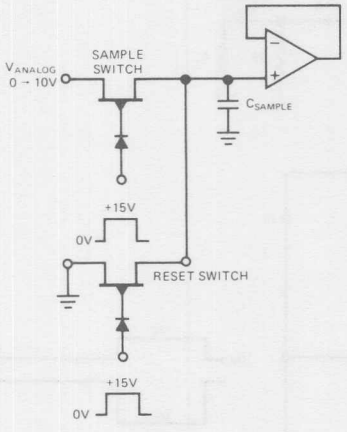


FIGURE 35. SAMPLE AND HOLD SWITCH

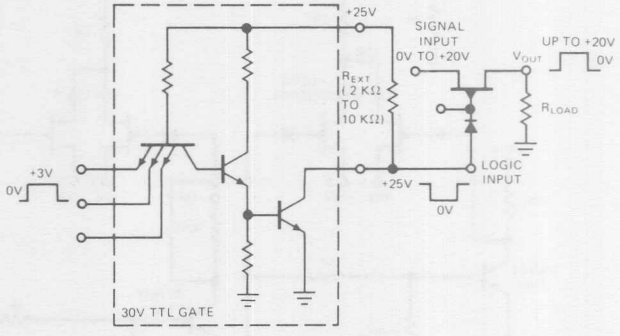
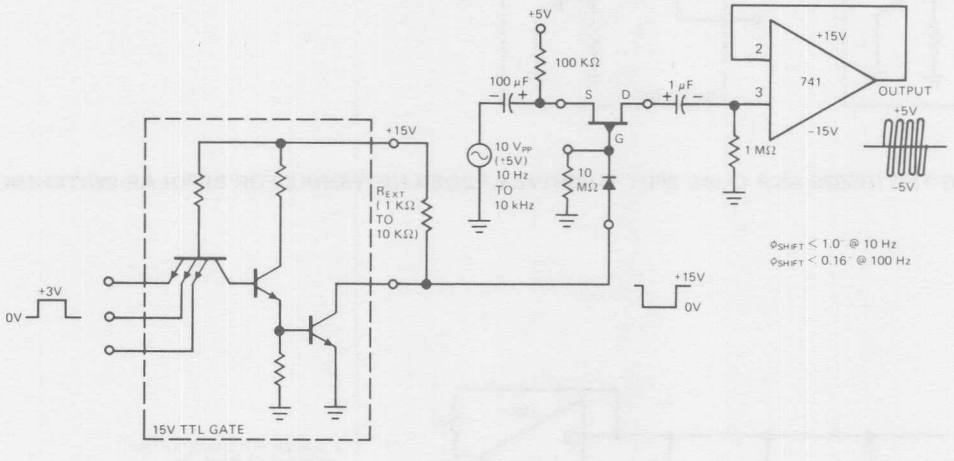
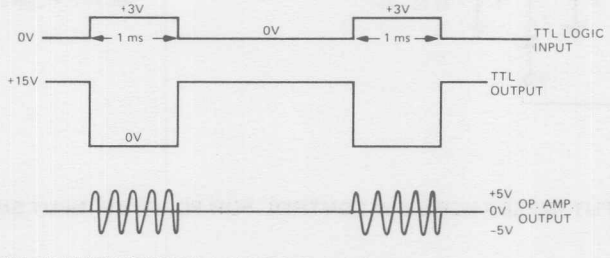


FIGURE 36. SWITCHING UP TO +20V SIGNALS WITH T^2L LOGIC





NOTE: TO SWITCH ±10 VAC ($20V_{pp}$): (1) INCREASE ±5V SUPPLY TO +10V.
(2) INCREASE TTL SUPPLY FROM +15V to +25V.

FIGURE 37. SWITCHING BIPOLAR SIGNALS WITH T^2L LOGIC (ALTERNATE METHOD)

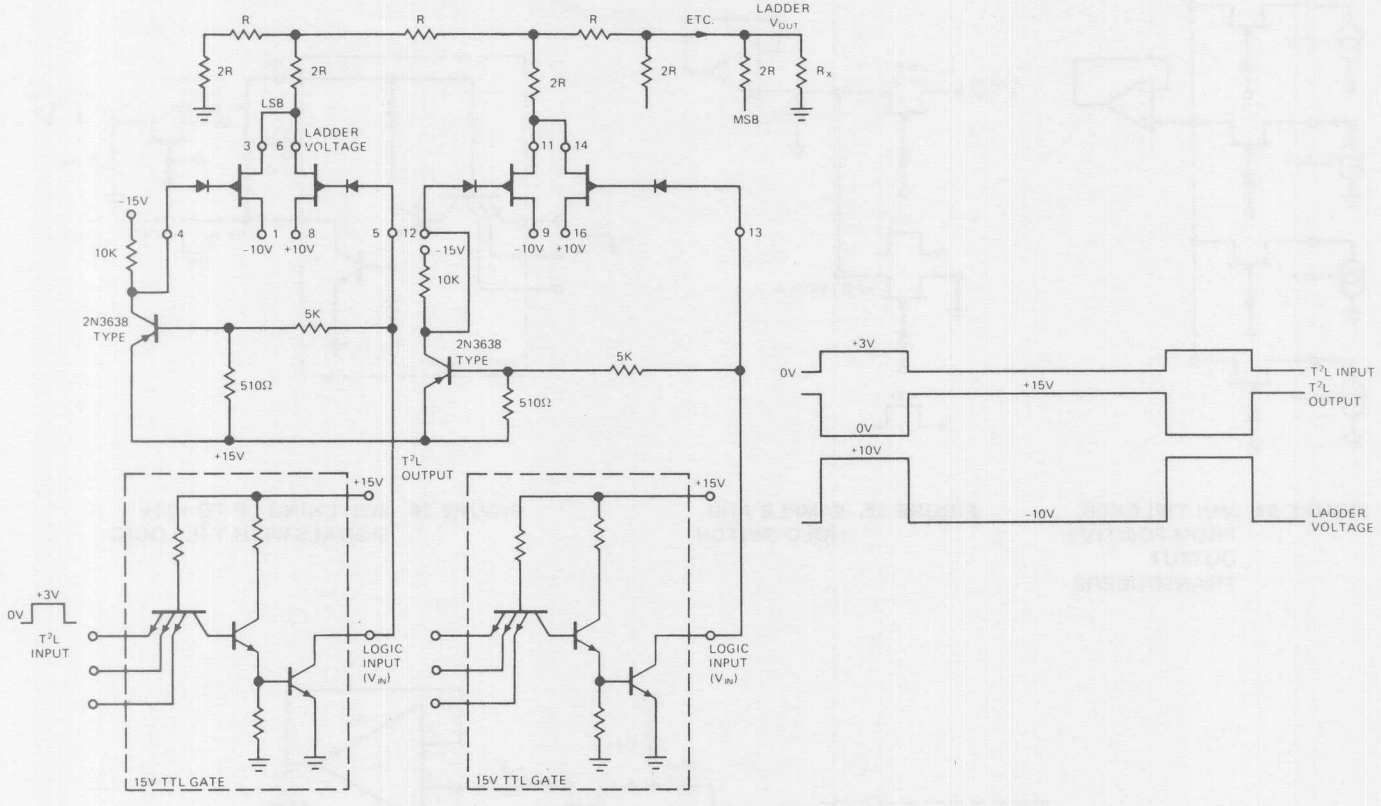
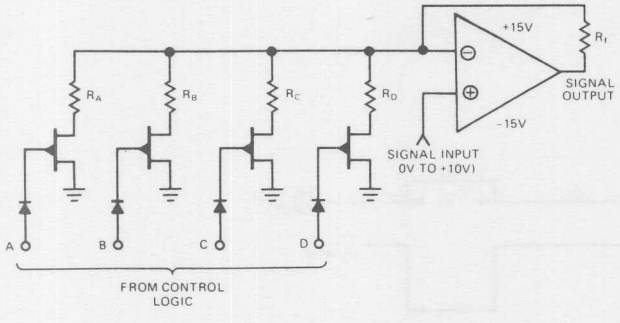


FIGURE 38. USING THE IH5028 AS A DUAL SPDT TO DRIVE LADDER NETWORKS FOR BI-POLAR SWITCHING (UP TO ±10V)



i.e. CHANGE B, C, D INPUTS = +15V;
CHANNEL A INPUT = 0V
∴ SIGNAL OUTPUT =

$$\frac{R_f + R_A}{R_A} \times \text{SIGNAL INPUT}$$

NOTE:
WHEN SWITCHING (+) OR ( ) SIGNAL INPUTS, A SCHEME SIMILAR TO FIGURES 10 OR 11 SHOULD BE USED.

FIGURE 39. HIGH INPUT IMPEDANCE GAIN CONTROL FOR POSITIVE INPUT SIGNALS USING IH5025.

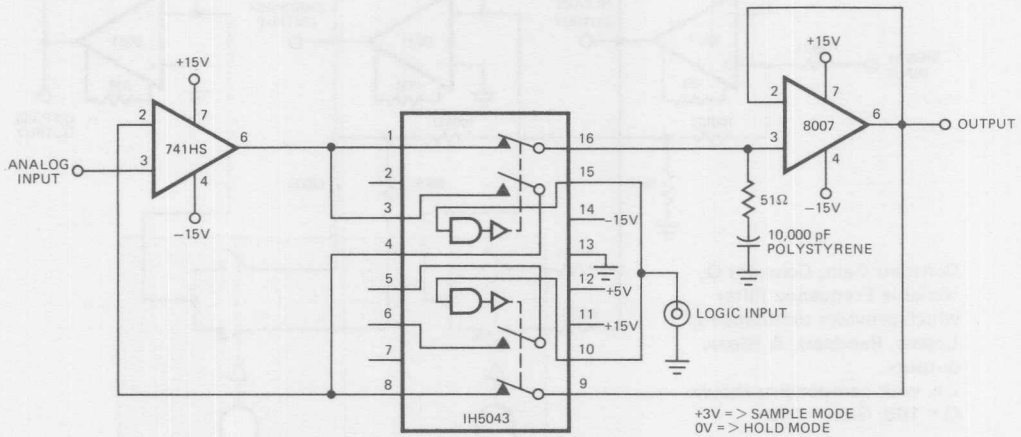


FIGURE 40. IMPROVED SAMPLE & HOLD USING IH5043
(NOTE: This circuit is available as a hybrid from Intersil.
Part number is IH5110/5111)

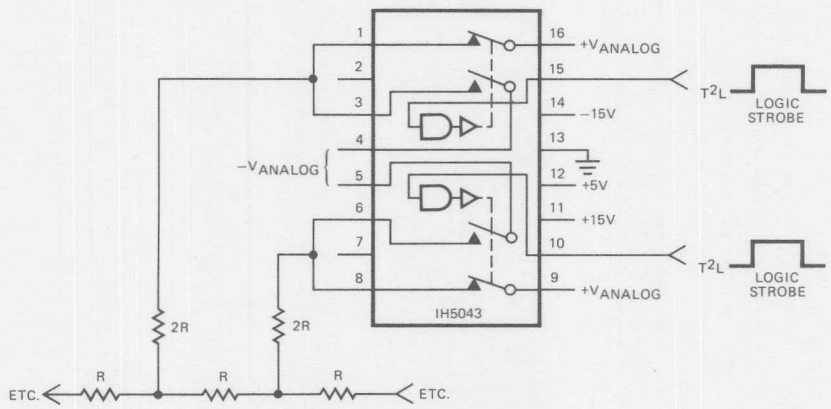
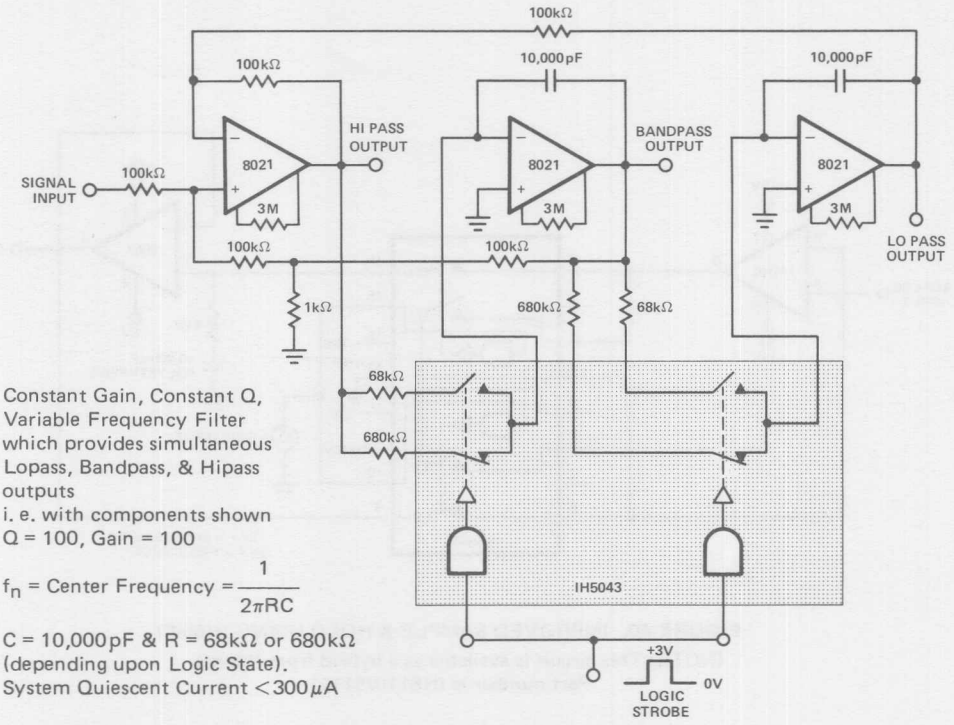


FIGURE 41. USING THE CMOS SWITCH TO DRIVE AN R/2R LADDER NETWORK (2 LEGS)

APPLICATIONS – IH5040 SERIES (Cont.)



Constant Gain, Constant Q,
Variable Frequency Filter
which provides simultaneous
Lopass, Bandpass, & Hipass
outputs
i. e. with components shown
Q = 100, Gain = 100

f_n = Center Frequency = $\frac{1}{2\pi RC}$

C = 10,000pF & R = 68kΩ or 680kΩ
(depending upon Logic State).
System Quiescent Current <300μA

FIGURE 42. DIGITALLY TUNED LOW POWER ACTIVE FILTER.